a second insulated gate transistor receiving the second voltage at a gate thereof and having a first conduction node connected to said first conduction node of said first insulated gate transistor, said second insulated gate transistor having a current supply ability different from a current supply ability of said first insulated gate transistor under a condition of the same gate voltage, and said difference signal corresponding to a difference between the first and second voltages;

operation current supply circuitry for supplying an operation current to the first and second insulated gate transistors, said operation current supply circuitry comprising a current mirror coupled to the first and second insulated gate transistors for supplying current to the first and second insulated gate transistors; and

a buffer circuit for buffering said difference signal for generating a binary level detection signal indicating whether said first voltage is higher than said second voltage.

Please cancel claim 21 in its entirety without prejudice or disclaimer of the subject matter thereof.

REMARKS

Claims 19-22 are presented for examination.

REJECTIONS UNDER 35 U.S.C. 112

Claims 19-22 have been rejected under 35 U.S.C. 112, first paragraph, as based on disclosure which is not enabling. Also, the claims have been rejected under 35 U.S.C. 112, second paragraph, as being indefinite.

The Examiner contends that it cannot be understood how the claimed arrangement will operate without the tail current source N22 of FIG. 4 or 8, which is not included in claim 19.

These rejections are respectfully traversed for the following reasons.

The current source transistor N22 is used for controlling activation of the differential amplifier that performs the differential amplification to detect the voltage difference. If the transistor N22 were not provided, the differential amplifier would be activated when the power is up.

Accordingly, the level detection circuitry of claim 19 would be able to detect a difference between the claimed first and second voltages without the transistor N22. Hence, the transistor N22 is not critical or essential for operation of the claimed level detection circuitry because this circuitry is able to operate without the transistor N22.

However, considering the Examiner's remarks, claim 19 has been amended to more clearly define the claimed invention.

In particular, claim 19, as amended, recites that the level detection circuitry comprises operation current supply circuitry for supplying an operation current to the first and second insulated gate transistors. The operation current supply circuitry comprises a current mirror coupled to the first and second insulated gate transistors for supplying current to the first and second insulated gate transistors. Also, the level detection circuitry comprises a buffer circuit for buffering the difference signal to generate a binary level detection signal indicating whether the first voltage is higher than the second voltage. Claim 21 reciting the buffer circuit has been cancelled.

It is believed that claims 19-20 and 22, as now amended, fully comply with the statutory requirement to set out and circumscribe a subject matter area with a reasonable degree of precision and particularity.

REJECTION UNDER 35 U.S.C. 102

Claims 19-22 have been rejected under 35 U.S.C. 102(b) as being anticipated by Kimura '226. The Examiner contends that FIG. 4 of the reference discloses all claimed elements.

Claim 19, as amended, recites a level detection circuitry for detecting a difference between a first voltage and a second voltage. The circuitry comprises a first insulated gate transistor receiving the first voltage at a gate thereof and having a first conduction node, and a second conduction node for outputting a difference signal; and a second insulated gate transistor receiving the second voltage at a gate thereof and having a first conduction node connected to the first conduction node of the first insulated gate transistor. The second insulated gate transistor has a current supply ability different from a current supply ability of the first insulated gate transistor under a condition of the same gate voltage. The difference signal corresponds to a difference between the first and second voltages. Operation current supply circuitry supplies an operation current to the first and second insulated gate transistors. The operation current supply circuitry comprises a current mirror coupled to the first and second insulated gate transistors for supplying current to the first and second insulated gate transistors. A buffer circuit buffers the difference signal for generating a binary level detection signal indicating whether the first voltage is higher than the second voltage.

Considering the reference, Kimura discloses the arrangement for compensating for temperature dependency of the low output voltage in the error amplifier, in which the mirror rate of the current mirror circuit is set to K2, and the rate of the transconductance β of the differential stage transistors is set to K2. The coefficients K1 and K2 are adjusted to adjust the temperature characteristics of the offset voltage in the error amplifier in accordance with the temperature characteristics of the transistors in the error amplifier for canceling the temperature dependency of the output voltage.

Kimura teaches producing the output voltage in accordance with output signal of the differential stage. While Kimura discloses that output signal of the differential stage is buffered to produce the output voltage, this output voltage is an analog voltage reflecting the voltage difference at the differential stage. Kimura merely considers compensation of the temperature dependent output voltage produced by the constant voltage generating circuit for generating a constant voltage in accordance with the reference voltage. Kimura fails to show the use of an error amplifier as a difference detection circuit.

By contrast, claim 19, as amended, requires the buffer circuit to generate a binary signal indicating whether the first voltage is higher than the second voltage. The reference does not teach or suggest the claimed buffer circuit.

It is noted that the Examiner's rejection of claims 19-22 under 35 U.S.C. 102 did not address claim 21 reciting the buffer circuit for generating a binary level detection signal indicating whether the first voltage is higher than the second voltage.

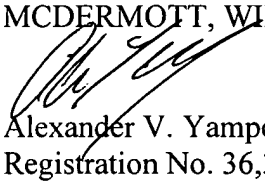
In view of the foregoing, and in summary, claims 19-20 and 22 are considered to be in condition for allowance. Favorable reconsideration of this application, as amended, is respectfully requested.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

MCDERMOTT, WILL & EMERY



Alexander V. Yampolsky
Registration No. 36,324

600 13th Street, N.W.
Washington, DC 20005-3096
(202)756-8000 AVY:vgp
Facsimile: (202)756-8087
Date: June 4, 2002

APPENDIX SHOWING CHANGES MADE

IN THE CLAIMS:

Claim 19 has been amended as follows:

19. (Amended) [A level] Level detection circuitry for detecting a difference between a first voltage and a second voltage, comprising:

a first insulated gate transistor receiving the first voltage at a gate thereof and having a first conduction node, and a second conduction node for outputting a difference signal;

a second insulated gate transistor receiving the second voltage at a gate thereof and having a first conduction node connected to said first conduction node of said first insulated gate transistor, said second insulated gate transistor having a current supply ability different from a current supply ability of said first insulated gate transistor under a condition of the same gate voltage, and said difference signal corresponding to a difference between the first and second voltages; [and]

operation current supply circuitry for supplying an operation current to the first and second insulated gate transistors, said operation current supply circuitry comprising a current mirror coupled to the first and second insulated gate transistors for supplying current to the first and second insulated gate transistors; and

a buffer circuit for buffering said difference signal for generating a binary level detection signal indicating whether said first voltage is higher than said second voltage.